IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 12, Issue 2, Ver. II (Mar.-Apr. 2017), PP 20-27
www.iosrjournals.org

Cmos Full Adder and Multiplexer Based Encoder for Low Resolution Flash Adc

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Abstract: *The present investigation proposed a low power encoding scheme of thermometer code to binary code converter for flash analog to digital conversion by the design of different circuits. In this paper, we have proposed three encoding techniques for the conversion of analog to digital signal using Multiplexer based encoder, heterogeneous encoder and encoding technique using dynamic logic circuits providing low power of operation and we compare the results obtained from each technique based on power consumption. The multiplexer based encoder was designed with the help of multiplexers which consumes less amount of power comparing with other designs.*

Keywords: *Analog to digital converter, Multiplexer based encoder, TIQ comparator, Heterogeneous encoder, Dynamic logic.*

I. Introduction

The flash ADC is a fastest speed compared to other ADC architectures. Therefore, it is mainly used for high speed and large bandwidth applications such as radar processing, digital oscilloscopes and so on. The flash ADC is also known as parallel ADC because of its parallel architecture. Analog to Digital Converter (ADC) plays an important role in digital signal processing systems. The main challenges of designing ADC for system on chip applications are high speed, low voltage, and low power consumption. Reducing the power consumption is a major concern in a portable device. Low power techniques are applied to prolong the battery life of a system. Similarly ADCs also require a low power technique in the design to reduce the total power consumption of ADC.Speed, power dissipation and resolution are the three crucial parameters the design of any ADC which cannot be changed once the design is complete. In wireless and mobile communication applications require a high speed ADC with low resolution. In these applications, flash ADC is the most suitable ADC because of its parallel operation. The complete conversion is done in a single cycle with the help of a large number of comparators. The below figure illustrates the structural design of a typical flash ADC. This architecture requires 2^n-1 comparators for the operation. For example if the circuit requires five bit as output then the number of comparators to be used was 31 as per calculation. The exponential increase of the number of comparators in flash ADC leads to a large die size as well as large power consumption in a chip. The reference voltage of each comparator is provided by an external reference source. The reference voltages are equally spaced between largest reference voltage and the smallest reference voltage. A common analog input is given to each and every individual comparator which are used in flash ADC. Since all the comparators are functioning in parallel way, the output is produced in a single cycle. The digital outputs which are obtained in a specific manner from the comparators are called thermocode and further there will be a encoder for converting the resulting thermocode to binary code. Here, in this paper the encoders designed for the conversion are multiplexer based encoder, heterogeneous encoder and dynamic logic using full adders.

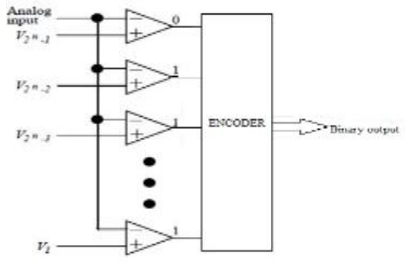


Fig. 1. Illustration of Flash ADC

The proposed encoder dynamic logic utilizes the properties of logic style implementation and Wallace tree implementation. In order to reduce the power dissipation the logic implementation is done with the use of dynamic logic. To make the code as more resilient i.e., lack of errors last stage was implemented using Wallace tree encoder. The present investigation was described as follows. The designing of three encoders explains in section 2. The method of implementation is described in the section3. Succeeding results, comparison and conclusion are provided.

II. Design Analysis Of The Propoed Encoders

The conversion from output of a comparator thermometer code to binary code is one of the bottlenecks in flash ADC. The bubble error usually results from timing differences between clock and signal lines and it is a situation where '1' is found above zero in thermometer code. The binary output totally depends on the output of a comparator based on number of '1's.If the number of '1's at the output was 'n' then the binary output code was 'n'. While designing thermometer code to binary code conversion two parameters are taken into consideration is error handling capability and power dissipation. Offset voltage in the comparator creates a bubble error in the thermometer code. Generally two methods are introduced to reduce the bubble errors. The first method is to convert thermometer code to gray code and then convert to binary code. But the accuracy of gray code steadily decreases as more number of comparators are used and more number of bubble errors is present in the thermometer code. The second method is the usage of Wallace tree encoder for the implementation using full adders for dynamic logic. This technique offers high robustness to bubble error and stuck at fault error because of its inherent global error correction or suppression capability. The disadvantage of this method is to provide a large delay of the encoder. In the first stage, conversion of thermometer code into two different four bit binary codes is done. With the help of four full adders and two different four bit binary codes, the final binary code was designed. The design equations which relates the thermometer code and binary code is presented and truth table is also shown below.

MUX and heterogeneous encoders was designed with the help of full adders and multiplexers where the binary output depends on the ONEs obtained from the comparators as described below.

DESIGN EQUATIONS:

$$b_3 = T_8$$

$$b_2 = T_4 \bullet \overline{T_8} + T_{12}$$

$$b_1 = T_2 \bullet \overline{T_4} + T_6 \bullet \overline{T_8} + T_{10} \bullet \overline{T_{12}} + T_{14}$$

$$b_0 = T_1 \bullet \overline{T_2} + T_3 \bullet \overline{T_4} + T_5 \bullet \overline{T_6} + T_7 \bullet \overline{T_8} + T_9 \bullet \overline{T_{10}} + T_{11} \bullet \overline{T_{12}} + T_{13} \bullet \overline{T_{14}} + T_{15}$$

$$a_3 = T_{24}$$

$$a_2 = T_{20} \bullet \overline{T_{24}} + T_{28}$$

$$a_1 = T_{16} \bullet \overline{T_{20}} + T_{22} \bullet \overline{T_{24}} + T_{26} \bullet \overline{T_{28}} + T_{30}$$

$$a_0 = T_{17} \bullet \overline{T_{18}} + T_{19} \bullet \overline{T_{20}} + T_{21} \bullet \overline{T_{22}} + T_{23} \bullet \overline{T_{24}} + T_{25} \bullet \overline{T_{26}} + T_{27} \bullet \overline{T_{28}} + T_{20} \bullet \overline{T_{30}} + T_{31}$$

B4	B3	B2	B1	B0	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	00000000000000000000000000000011
0	0	0	1	1	00000000000000000000000000000111
0	0	1	0	0	00000000000000000000000000001111
0	0	1	0	1	00000000000000000000000000011111
0	0	1	1	0	00000000000000000000000000111111
0	0	1	1	1	00000000000000000000000001111111
0	1	0	0	0	00000000000000000000000011111111
0	1	0	0	1	00000000000000000000000111111111
0	1	0	1	0	00000000000000000000001111111111
0	1	0	1	1	00000000000000000000011111111111
0	1	1	0	0	00000000000000000000111111111111
0	1	1	0	1	00000000000000000001111111111111
0	1	1	1	0	00000000000000000011111111111111
0	1	1	1	1	00000000000000000111111111111111
1	0	0	0	0	00000000000000001111111111111111
1	0	0	0	1	00000000000000011111111111111111
1	0	0	1	0	00000000000000111111111111111111
1	0	0	1	1	00000000000001111111111111111111
1	0	1	0	0	00000000000011111111111111111111

1	0	1	0	1	00000000001111111111111111111111
1	0	1	1	0	00000000011111111111111111111111
1	0	1	1	1	00000000111111111111111111111111
1	1	0	0	0	00000001111111111111111111111111
1	1	0	0	1	00000011111111111111111111111111
1	1	0	1	0	00000111111111111111111111111111
1	1	0	1	1	00001111111111111111111111111111
1	1	1	0	0	00011111111111111111111111111111
1	1	1	0	1	00111111111111111111111111111111
1	1	1	1	0	01111111111111111111111111111111
1	1	1	1	1	11111111111111111111111111111111

Table- Thermometer to binary code converter.

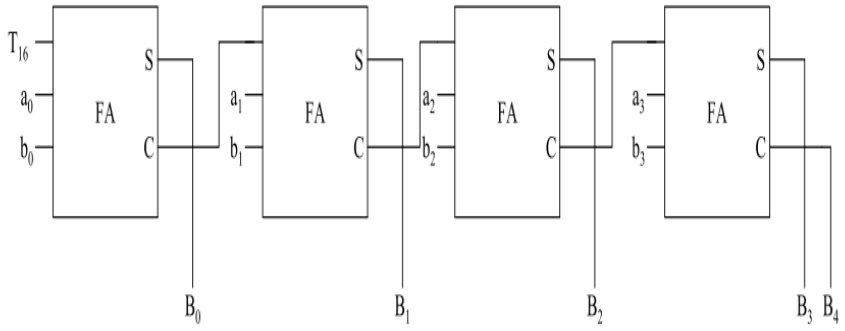


Fig. 2 Final Stage Implementation using Full Adders

2.1 TIQ COMPARATOR

In N bit Flash ADC 2^N-1 comparator is employed to compare the reference voltage with the input voltage to induce the thermometer code. Generally, resistor ladder is employed to generate reference voltage. This design is complex and additionally consumes more power and area. So in this paper we have proposed a comparator based on Threshold Inverter Quantization(TIQ) technique which is alternative approach to reduce the power consumption and chip area, it is basic CMOS inverter consists of one PMOS and one NMOS transistor with the switching threshold voltage.TIQ comparator made up of two cascade CMOS inverter where the first inverter is used to set the reference voltage of comparator by varying the parameters like width and length of PMOS and NMOS transistors where as the second inverter increases the voltage gain and manage linearity balance for the voltage rising and falling intervals of high frequencies input signals.

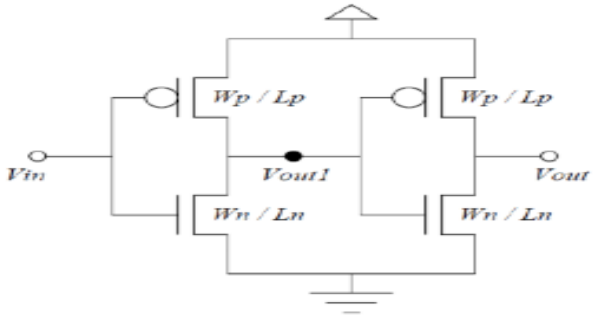
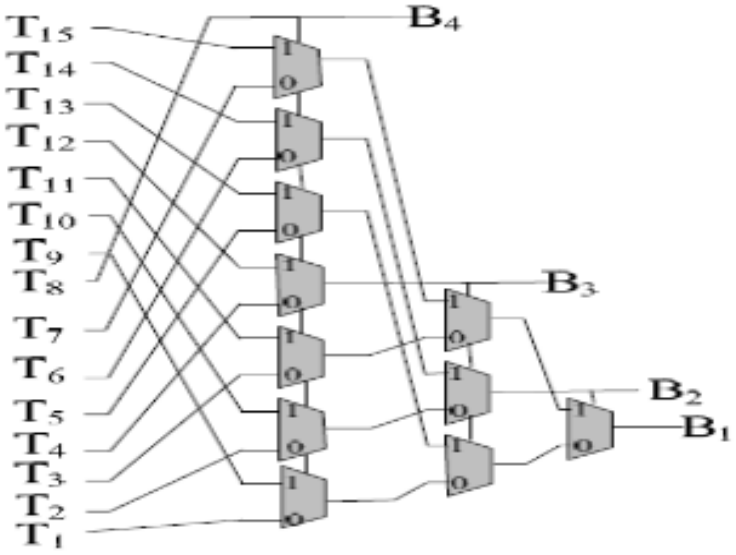


Fig:TIQ comparator

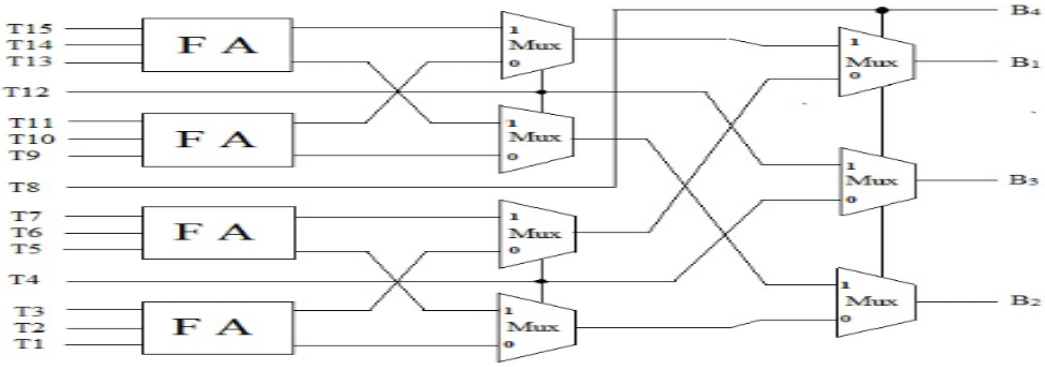
2.1.1 MULTIPLEXER ENCODING TECHNIQUE

MUX based encoders operates at high speed and covers the small chip area compared to the dynamic logic encoding technique. This encoder is implemented by grouping the results of smaller length MUX based encoder to develop a high bit resolution encoder to convert thermometer code into binary output. It gives better result than previous encoders in terms of power consumption, speed and space.



2.1.2 HETEROGENEOUS ENCODER

Heterogeneous encoder can be implemented by using any one of the existing encoders like Wallace tree encoder and multiplexer based encoder. This encoder was designed using full adders and multiplexers as shown below. In this selection signal is used from MUX which is critical. This can tolerant the bubble error and remaining signal can be used as inputs. Wallace encoder is also free from bubble error but the circuit is complex in nature. Hence, this encoder is designed which is easy to implement and also consumes less power.



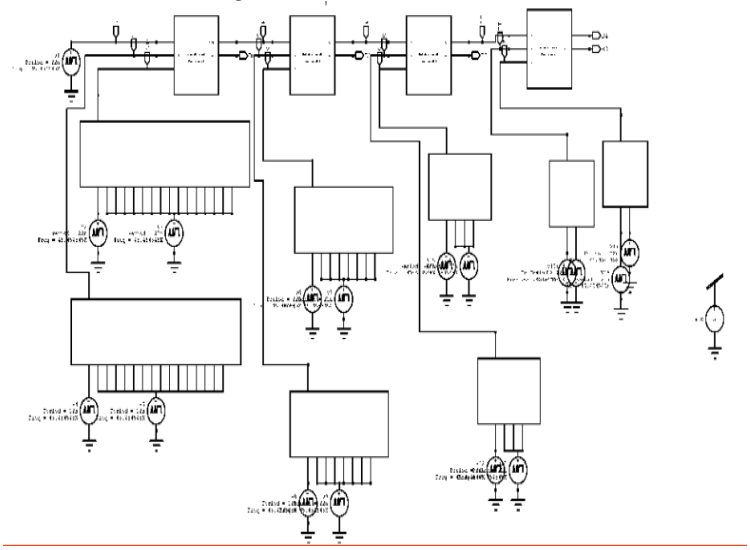
III. Implementation Of Proposed Encoders

In order to convert the thermometer code to binary code different methods are implemented based on design equations. Pseudo NMOS, static CMOS and dynamic logic are the methods implemented for the conversion. One of the proposed encoding technique was dynamic logic as it overcome the disadvantages of other two methods. Since the power dissipation, consumption and number of transistors used was high for those two methods. Based on this intention, we proposed an encoding technique by dynamic logic providing low power consumption and medium speed of operation.

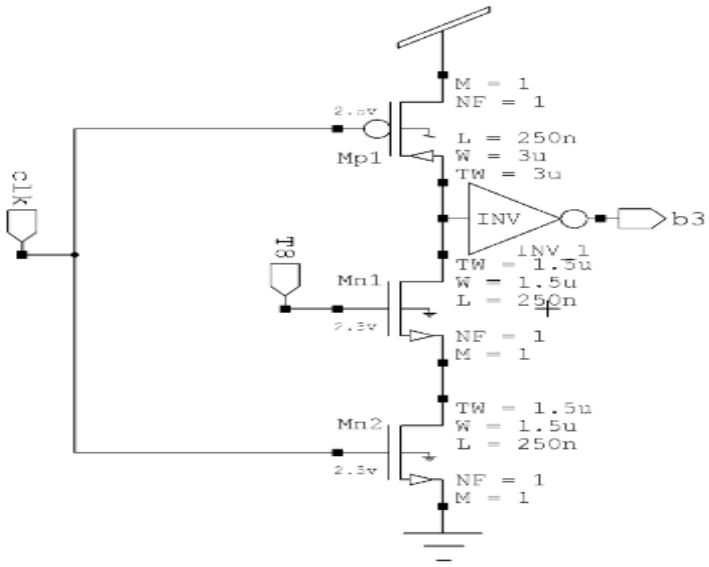
The operation of dynamic logic evaluates in two phases namely precharge and evaluation. During precharging phase, when CLK=0, the output mode is fully charged to supply voltage vdd irrespective of pull down network through pull up transistor. At this time, the pull down path is disconnected as CLK is connected directly to NMOS transistor. The next phase is evaluation is done when CLK=1. In this case the pull up transistor is disconnected from the circuit and pull down path is discharged conditionally based on different inputs given to the circuit.

The main thing to be concerned was during evaluation phase, the input to the gate has to make atmost one transition. The schematic implementation of dynamic logic, MUX based encoders and heterogeneous encoder are shown below.

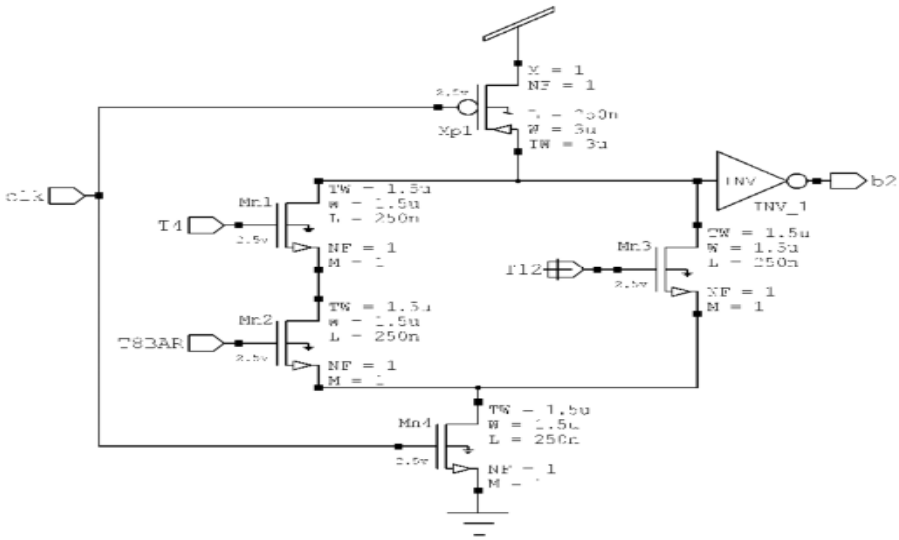
3.1 PROPOSED ENCODING TECHNIQUE USING DYNAMIC LOGIC



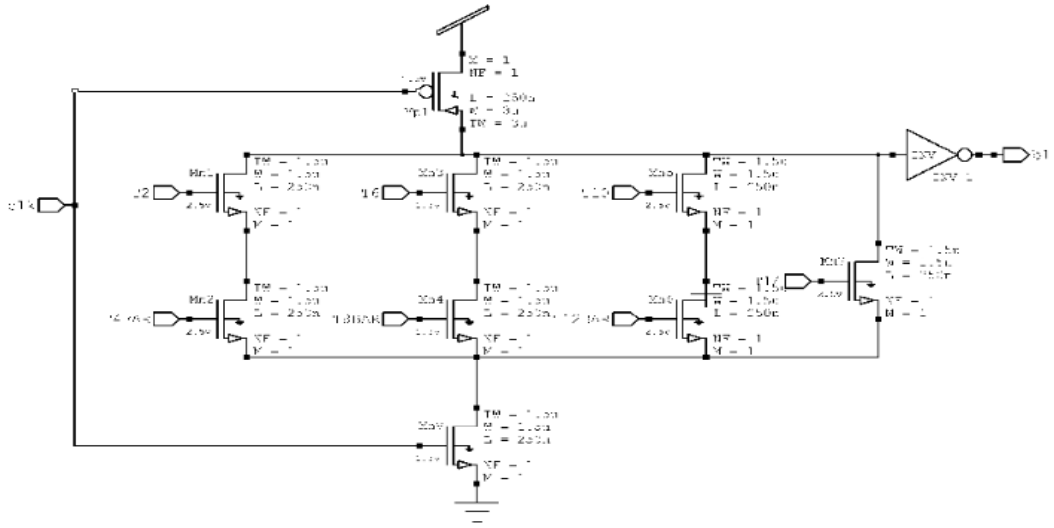
3.1.1 IMPLEMENTATION OF b3



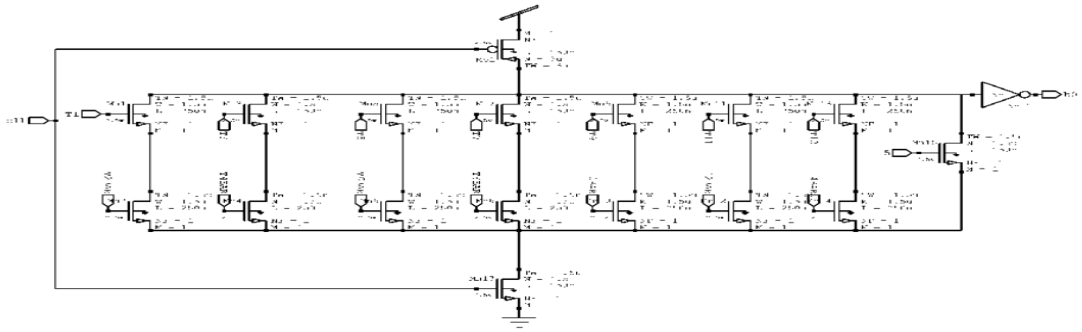
3.1.2 IMPLEMENTATION OF b2



3.1.3 IMPLEMENTATION OF b1

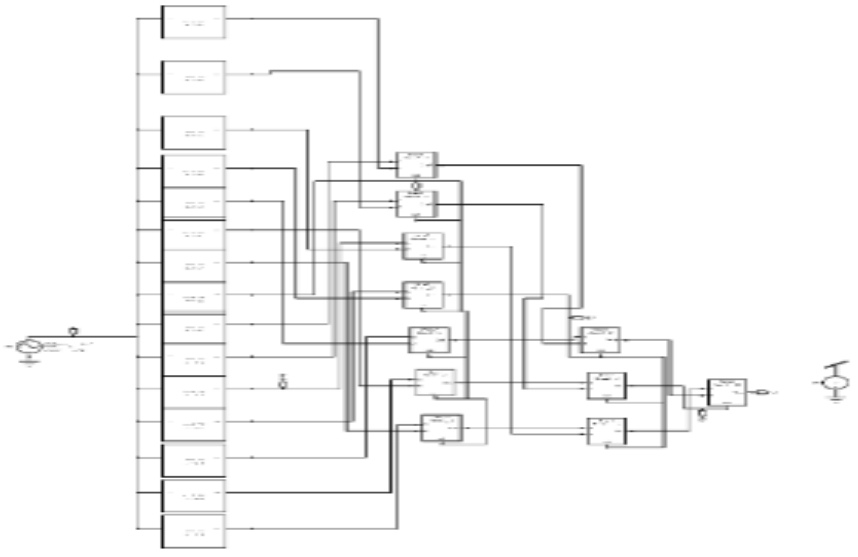


3.1.4 IMPLEMENTATION OF b0



3.2 MULTIPLEXER BASED ENCODER

The operation of multiplexer based encoder is as follows. The input signal is given to the TIQ comparator as a sinusoidal and it compares it with the threshold voltage generated by the first cmos invereter of comparator and generates the output signal as binary generating a thermometer code from all comparators. The output of each comparator is given to multiplexers in which each cell counts number of logical ONEs at each entries performing operation and generates a final binary output.

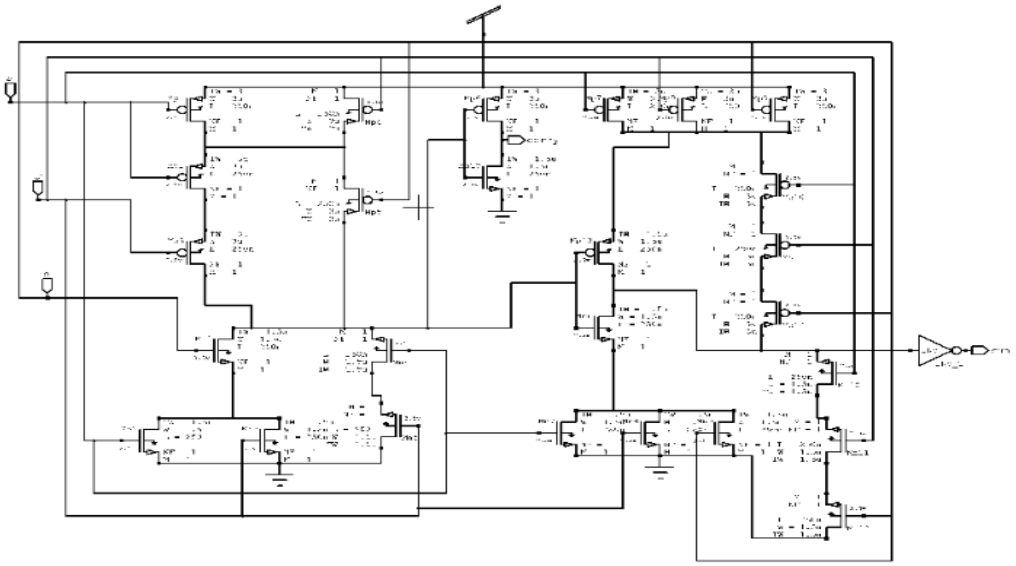


3.2.1 IMPLEMENTATION OF CMOS FULL ADDER

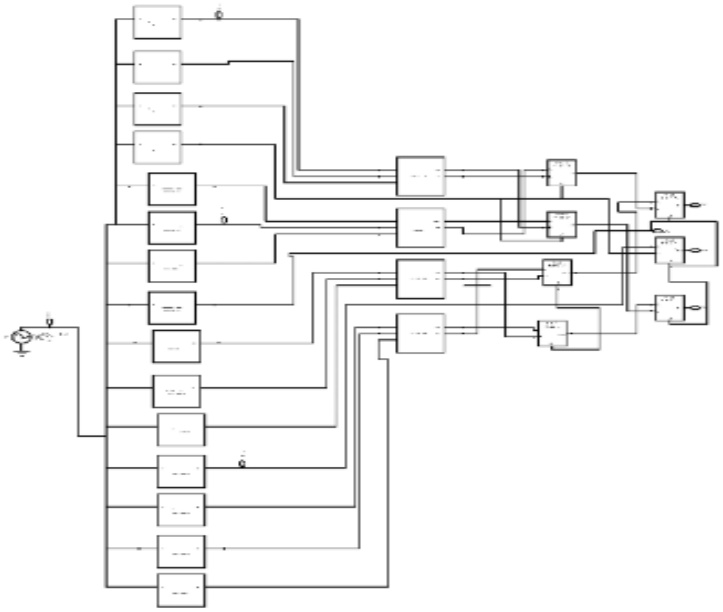
We have designed a CMOS full adder which consists of 28 transistors which consumes less amount of power and the design equation is as follows

sum= a xor b xor c

carry=$\overline{b(a \text{ xor } c)\ ac}$



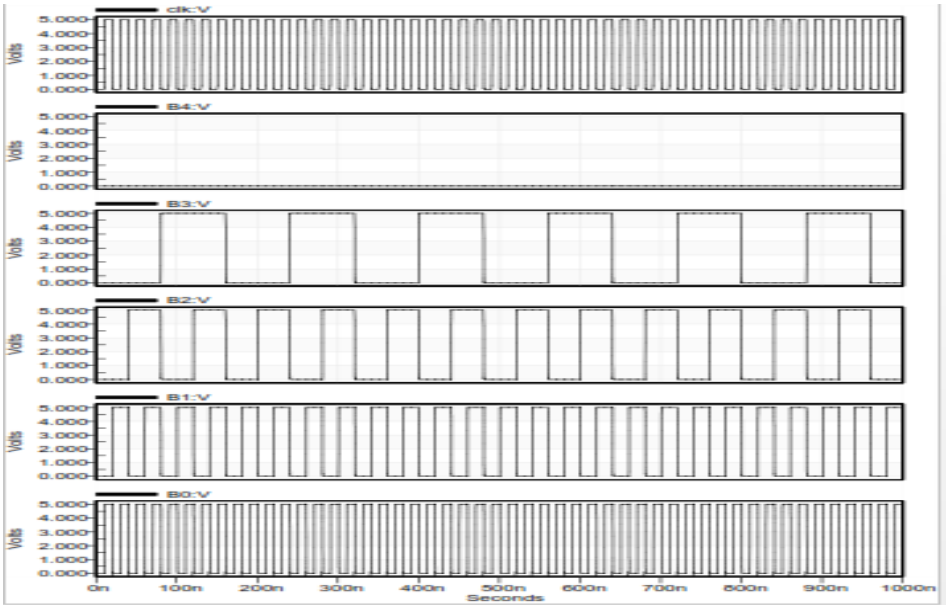
3.3 HETEROGENEOUS BASED ENCODER



IV. Simulation Results

The proposed encoders which are designed had been tested for every inputs given in the truth table and results were verified. Three types of encoders used in this paper were compared based on the results obtained from power analysis. The MUX based encoder consumes less power for operation comparing with dynamic logic and heterogeneous encoders as shown in the table. The reconfigurable capability of the proposed encoders makes the design adaptable to reconfigurable flash ADC architecture.

4.1 SIMULATED OUTPUT



4.2 COMPARISON TABLE:

Results	Dynamic logic	Heterogenous encoder	MUX based encoder
Architecture	Flash	Flash	Flash
Resolution	5 bits	4 bits	4 bits
Vdd	5 V	5 V	5 V
Power consumption	0.9415mw	1.08mW	0.8479mW

V. Conclusion

Now a days the growth of portable device and battery operated like cell phone, laptops has increased. Hence the device should be designed which consumes less power and have minimal area and device can be operated for long time. TIQ removes the array of resistors that makes the ADC devices to operate faster and takes less area. Hence we have designed three encoding techniques in which a MUX based encoder for the binary conversion which consumes less amount of power compared to the other techniques based on above results

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